WHAT IS CLAIMED IS:

1. A method of executing an instruction comprising:

receiving residual data of a first image and decoded pixels of a second image;

zero-extending a plurality of unsigned data operands of the decoded pixels producing a plurality of unpacked data operands;

adding a plurality of signed data operands of the residual data to the plurality of unpacked data operands producing a plurality of signed results;

saturating the plurality of signed results producing a plurality of unsigned results.

2. The method as recited in Claim 1, wherein the residual data comprises data results from an inverse discrete cosine transform (DCT) operation and the second image comprises a previously decoded video frame.

3. The method as recited in Claim 1, wherein the second image is an earlier decoded block from a same video frame as the first image.

4. The method as recited in Claim 1, wherein the zero-extending, the adding and the saturating are part of a video estimation function.

5. The method as recited in Claim 1, wherein the zero-extending, the adding and the saturating are part of a video compensation function.

6. The method as recited in Claim 1, wherein the instruction is a Single-Instruction/Multiple-Data (SIMD) instruction.

7. The method as recited in Claim 1, wherein the method comprises executing a Single-Instruction/Multiple-Data (SIMD) instruction.

8. The method as recited in Claim 1, wherein the method is performed utilizing Single-Instruction/Multiple-Data (SIMD) circuitry.

9. A method comprising:

decoding an instruction identifying a mixed-mode addition operation;

executing the instruction on a first source and a second source, wherein the first source comprises a plurality of signed residual data of a first image and the second source comprises a plurality of unsigned decoded pixels of a second image; and

storing an output of the executing the instruction, wherein the output comprises a plurality of unsigned result pixels;

wherein the executing the instruction comprises:

zero-extending at least one of the plurality of unsigned decoded pixels;

adding the at least one of the plurality of unsigned decoded pixels and the plurality of signed residual data producing a plurality of signed sums; and

saturating the plurality of signed sums producing the plurality of unsigned result pixels.

10. The method as recited in Claim 9, further comprising:

executing the instruction on a third source and at least one other of the plurality of unsigned decoded pixels of the second source, wherein the third source comprises another plurality of signed residual data, wherein the executing produces another plurality of unsigned result pixels;

storing the another plurality of unsigned result pixels; and

performing an OR operation on the plurality of unsigned result pixels and the another plurality of unsigned result pixels, and storing a plurality of OR results into a single destination register.

11. The method as recited in Claim 9, wherein the plurality of signed residual data comprises data results from an inverse discrete cosine transform (DCT) operation and the second image comprises a previously decoded video frame.

12. The method as recited in Claim 9, wherein the zero-extending, the adding and the saturating are part of a video compensation function.

13. The method as recited in Claim 9, wherein the instruction is a Single-Instruction/Multiple-Data (SIMD) instruction.

14. An apparatus comprising:

a first plurality of multiplexers, each multiplexer of the first plurality of multiplexers operative to select one of a plurality of unsigned decoded pixels and zero-extend the unsigned decoded pixels, the first plurality of multiplexers operative to produce a plurality of unpacked operands;

a plurality of adders, each adder of the plurality of adders operative to add a signed residual data operand to one of the plurality of unpacked operands, the plurality of adders operative to produce a plurality of sums,

a plurality of saturation units operative to produce a plurality of unsigned result pixels from the plurality of sums.

15. The apparatus as recited in Claim 14, further comprising:

a second plurality of multiplexers operative to select between the plurality of unsigned result pixels and zeroes.

16. The apparatus as recited in Claim 14, wherein the plurality of adders comprises four 16-bit adders.

17. The apparatus as recited in Claim 14, wherein selection controls for the first plurality of multiplexers is according to a qualifier specified in a Single-Instruction/Multiple-Data (SIMD) instruction.

18. The apparatus as recited in Claim 14, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction.

19. The apparatus as recited in Claim 14, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

20. The apparatus as recited in Claim 14, wherein the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units form a Single-Instruction/Multiple-Data (SIMD) instruction execution circuit.

21. The apparatus as recited in Claim 14, wherein the signed residual data operand comprises data results from an inverse discrete cosine transform (DCT)

operation and the unsigned decoded pixels comprise a portion of a previously decoded video frame.

22. The apparatus as recited in Claim 21, wherein the apparatus is utilized by a video compensation function.

23. An apparatus comprising:

a coprocessor interface unit to identify an instruction for a mixed-mode operation, a first source having a plurality of signed residual data operands and a second source having a plurality of unsigned decoded pixels;

an execution unit to perform the mixed-mode operation on the plurality of signed residual data operands and the plurality of unsigned decoded pixels; and

a register to store a result having a plurality of unsigned result pixels;

wherein the execution unit comprises:

a first plurality of multiplexers, each multiplexer of the first plurality of multiplexers operative to select one of the plurality of unsigned decoded pixels and zero-extend the unsigned decoded pixels, the first plurality of multiplexers operative to produce a plurality of unpacked operands;

a plurality of adders, each adder of the plurality of adders operative to add one of the plurality of signed residual data operands and one of the plurality of unpacked operands, the plurality of adders operative to produce a plurality of signed sums, and

a plurality of saturation units operative to produce a plurality of unsigned result pixels from the plurality of signed sums.

24. The apparatus as recited in Claim 23, the execution unit further comprising:

a second plurality of multiplexers operative to select between the plurality of unsigned result pixels and zeroes.

25. The apparatus as recited in Claim 23, wherein the plurality of adders comprises four 16-bit adders.

26. The apparatus as recited in Claim 23, wherein selection controls for the first plurality of multiplexers is according to a qualifier specified in a Single-Instruction/Multiple-Data (SIMD) instruction.

27. The apparatus as recited in Claim 23, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction.

28. The apparatus as recited in Claim 23, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

29. The apparatus as recited in Claim 23, wherein the signed residual data operands comprise data results from an inverse discrete cosine transform (DCT) operation and the unsigned decoded pixels comprise a portion of a previously decoded video frame.

30. A data processing system comprising:

an addressable memory to store an instruction for a mixed-mode operation;

a processing core coupled to the addressable memory, the processor core comprising:

an execution core to access the instruction;

a first source register to store a plurality of signed residual data operands;

a second source register to store a plurality of unsigned decoded pixels; and

a destination register to store a plurality of unsigned result pixels;

a wireless interface to receive an encoded bit stream; and

an I/O system and decoder to provide the plurality of signed residual data operands to the first source register from the encoded bit stream;

wherein the execution core comprises:

a first plurality of multiplexers, each multiplexer of the first plurality of multiplexers operative to select one of the plurality of unsigned decoded pixels and zero-extend the unsigned decoded pixels, the first plurality of multiplexers operative to produce a plurality of unpacked operands;

a plurality of adders, each adder of the plurality of adders operative to add a signed residual data operand to one of the unpacked operands, the plurality of adders operative to produce a plurality of sums, and

a plurality of saturation units operative to produce a plurality of unsigned result pixels.

31. The data processing system as recited in Claim 30, wherein the plurality of adders comprises four 16-bit adders.

32. The data processing system as recited in Claim 30, wherein the I/O system and decoder comprise an inverse discrete cosine transform function.

33. The data processing system as recited in Claim 30, wherein selection controls for the first plurality of multiplexers is according to a qualifier specified in a Single-Instruction/Multiple-Data (SIMD) instruction.

34. The data processing system as recited in Claim 30, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction.

35. The data processing system as recited in Claim 30, wherein configuration of the first multiplexer, the adders, and the saturation units is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

36. The data processing system as recited in Claim 30, wherein the signed residual data operands comprise data results from an inverse discrete cosine transform (DCT) operation and the unsigned decoded pixels comprise a portion of a previously decoded video frame.